UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,920	12/28/2001	Juan G. Revilla	10559-566001 P12728	3816

20985 7590 02/23/2004

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA, 92130-2081

EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	9

DATE MAILED: 02/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,920	REVILLA ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *paper #7(10/20/03)*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/040,920

Art Unit: 2186

Part III DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicant's communication filed December 17, 2003. This amendment has been entered and carefully considered. Claims 1-31 remain pending in the application. Claim 32 is newly added.

2. Applicant's arguments with respect to claims 1-31 have been considered but are not deemed to be persuasive.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-6, 11-13, 15-20 and 32 are rejected under 35 U.S.C. § 102(e) as being anticipated by Arimilli et al., hereinafter Arimilli (USPN: 6,405,289);

As per claims 1 and 11; Arimilli discloses the invention as claimed including a method comprises receiving a request for access to a memory location (e.g. see column 3, line 16 et seq.); examining a local memory descriptor associated with the memory block (e.g. see column 3, line 17), and accessing a local addressable memory in response to the local memory descriptor indicating that the memory block is in the local addressable memory is embedded in the system of Arimilli since this concept is equivalent to polling the cache (detailed on column 3, lines 17 et seq.) by comparing the tag address which yields a tag hit;

As per claim 2, Arimilli discloses accessing the memory location in response to the memory location existing in the local addressable memory (e.g. see column 3, lines 37-41);

As per claim 3, generating an illegal access violation exception in response to the memory location not existing in the local addressable memory is equivalent to MISS condition when polling L1 cache and the request being forwarded to the L1 cache (30) or higher memory in the hierarchy (e.g. see column 3, lines 17 et seq.);

As per claim 4, Arimilli discloses accessing a local cache in response to the local memory descriptor indicating that the

memory block is not in the local addressable memory (e.g. see column 3, lines 17 et seq.);

As per claims 5 and 6, the further limitation of receiving request for access to a memory location comprises receiving an address and identifying a page having an address space including the address is embedded in the system of Arimilli, especially in cache polling or cache memory access, since address must be presented to tag unit for comparison to determined hit or miss condition (e.g. see column 3, lines 17 et seq.);

As per claim 12; Arimilli discloses accessing the local addressable memory by polling its internal L1 cache (e.g. see column 3, lines 17 et seq.);

As per claim 13; generating an illegal access violation exception in response to the memory location not existing in the local addressable memory is equivalent to MISS condition when polling L1 cache and the request being forwarded to the L1 cache (30) or higher memory in the hierarchy (e.g. see column 3, lines 17 et seq.);

As per claims 15-18 and 19-20, they encompass the same scope of invention as to that of claims 1-10 and 11-14 except that they are drafted as apparatus format rather than method format, the claims are therefore rejected for the same reasons as being set forth above.

As per claim 32; Arimilli discloses the invention as claimed

including a method comprises receiving a request for access to a memory location (e.g. see column 3, line 16 et seq.); examining a local memory descriptor associated with the memory block (e.g. see column 3, line 17), and accessing a local addressable memory in response to the local memory descriptor indicating that the memory block is in the local addressable memory is embedded in the system of Arimilli since this concept is equivalent to polling the cache by comparing the tag address which yields a tag hit (detailed on column 3, lines 17 et seq.); accessing local cache in response to the local memory descriptor indicating that the memory block is not in the local addressable memory is equivalent taught as when attempting to read a memory block which is not present in the local addressable memory L1, the request is forwarded to cache 30 in response to L1 poll (local descriptor) (e.g. see column 3, lines 18-19).

Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7-10, 14 and 21-31 are rejected under 35

U.S.C. 103(a) as being unpatentable over Arimilli et al., hereinafter Arimilli (USPN: 6,405,289);

As per claims 7-10, and 14; Arimilli discloses memory status/descriptor bit wherein the cache coherence protocol associates with each block in each level of the cache hierarchy, a status indicator indicating the current state of the block, the state information is used to allow certain optimizations in the coherency protocol for reducing message traffic on the generalized interconnect and the inter-cache connection (e.g. see column 4, lines 1 et seq.); in addition, referring to the MESI protocol wherein each cache memory block is associated with different block state of MESI(e.g. see column 4, lines 28 et seq.). Arimilli; however, does not particularly discloses the cache memory being implemented as SRAM type of cache memory wherein SRAM bit can be implemented as being claimed. First of all, it should be noted that SRAM is a commonly-known cache implementation; secondly, Applicant neither disclosing in the specification nor claiming in the current invention that different type of cache would change or vary the operation of system. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement Arimilli's cache as SRAM type of cache, since SRAM cache is known in the art as cheaper than most other type of memories; in addition, by implementing cache memory as SRAM type,

memory refresh is not required, therefore being advantageous.

As per claims 21-27; Arimilli discloses the invention as claimed, detailed above with respect to claims 1-20 and 28-29; Arimilli however does not particularly disclose a computer-readable medium of instructions to be implemented on a computer as being claimed in claims 7-12. However, one of ordinary skill in the art would have recognized that computer readable medium (i.e., floppy, cd-rom, etc.) carrying computer-executable instructions for implementing a method, because it would facilitate the transporting and installing of the method on other systems, is generally well-known in the art. For example, a copy of the Microsoft Windows operating system can be found on a cd-rom from which Windows can be installed onto other systems, which is a lot easier that running a long cable or hand typing the software onto another system. The examiner takes Official Notice of this teaching. Therefore, it would have been obvious to put Arimilli's program on a computer readable medium, because it would facilitate the transporting, installing and implementing of Arimilli's program on other systems.

As per claims 28-29 and 30-31; see arguments with respect to independents claims 1, 11 and 28 under 35 U.S.C. § 102(e) (paragraph 4); in addtition, referring to rejection of claims 7-10 and 14 for the SRAM implementation and 21-27 for computer-readable medium concept as being detailed above.

7. As per remark, Applicant's counsel contended that (a) Arimilli does not teach or suggest "accessing a local addressable memory in response to the local memory descriptor indicating that the memory block is in the local addressable memory" (see amendment's page 11, last paragraph); (b) Arimilli also does not teach or suggest "routing the request to one of a local addressable memory and a local cache in response to the state of a local descriptor associated with said memory block" (page 12, third paragraph).

With respect to (a) First of all, Examiner would like to emphasize that Arimilli discloses multilevel hierarchical cache memory having different local levels L1, L2 and L3 caches (e.g. see figures 1 and 4), wherein one of the local level caches (L1 or L2) can be considered to be equivalent to the claimed local addressable memory; secondly, the concept of accessing the local addressable memory being contended by Applicant's counsel is equivalent to the polling operation which yields cache hit or local memory hit; this concept is clearly taught by Arimilli starting on column 3, lines 17 et seq.; even though, Arimilli merely discloses if the memory block is not present in the L1 cache, the request is forwarded to the L2 cache; it would be clearly understood that the requested data or memory block would be accessed and retrieved, if it is present in the L1 cache after the hit result of the polling operation. By this rationale,

Examiner wholeheartly disagree with Applicant's counsel and believe Armilli clearly discloses and teaches all the limitations as recited in independent claim 1.

With respect to (b), Examiner would like to emphasize the the routing of the request to one of a local addressable memory and a local cache in response to the state of a local descriptor associated with said memory block is taught by Arimilli as the coherency protocol detailed on column 3, lines 23-42, wherein the request is routed to the local L1 cache memory (local addressable memory) for the modified data if the L1 cache having the modified copy of the requested data block.

8. Applicant's arguments filed December 17, 2003 have been fully considered but they are not deemed to be persuasive.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

10. Any inquiry concerning this communication or earlier

communications from the examiner should be directed to Tuan V. Thai whose telephone number is (703) 305-3842. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (703)-305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov.*** Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/February 20, 2004

Tuan V. Thai
PRIMARY EXAMINER
Group 2100